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UNITED STATES PATENT APPLICATION

FOR

DISPLAY SYSTEM HAVING IMPROVED MULTIPLE MODES FOR DISPLAYING IMAGE DATA FROM MULTIPLE INPUT SOURCE FORMATS

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DISPLAY SYSTEM HAVING IMPROVED MULTIPLE MODES FOR DISPLAYING IMAGE DATA FROM MULTIPLE INPUT SOURCE FORMATS

RELATED APPLICATIONS

[01] The present application is related to commonly owned (and filed on even date) United States Patent Applications: (1) United States Patent Application Serial No. {Attorney Docket No. 08831-0062} entitled "SYSTEM AND METHOD FOR PERFORMING IMAGE RECONSTRUCTION AND SUBPIXEL RENDERING TO EFFECT SCALING FOR MULTI-MODE DISPLAY", which is hereby incorporated herein by reference in its entirety.

BACKGROUND

[02] In commonly owned United States Patent Applications: (1) United States Patent Application Serial No. 09/916,232 ("the '232 application"), entitled "ARRANGEMENT OF COLOR PIXELS FOR FULL COLOR IMAGING DEVICES WITH SIMPLIFIED ADDRESSING," filed July 25, 2001; (2) United States Patent Application Serial No. 10/278,353 ("the '353 application"), entitled "IMPROVEMENTS TO COLOR FLAT PANEL DISPLAY SUB-PIXEL ARRANGEMENTS AND LAYOUTS FOR SUB-PIXEL RENDERING WITH INCREASED MODULATION TRANSFER FUNCTION RESPONSE," filed October 22, 2002; (3) United States Patent Application Serial No. 10/278,352 ("the '352 application"), entitled "IMPROVEMENTS TO COLOR FLAT PANEL DISPLAY SUB-PIXEL ARRANGEMENTS AND LAYOUTS FOR SUB-PIXEL RENDERING WITH SPLIT BLUE SUB-PIXELS," filed October 22, 2002; (4) United States Patent Application Serial No. 10/243,094 ("the '094 application), entitled "IMPROVED FOUR COLOR ARRANGEMENTS AND EMITTERS FOR SUB-PIXEL RENDERING," filed September 13, 2002; (5) United States Patent Application

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Serial No. 10/278,328 ("the '328 application"), entitled "IMPROVEMENTS TO COLOR FLAT PANEL DISPLAY SUB-PIXEL ARRANGEMENTS AND LAYOUTS WITH REDUCED BLUE LUMINANCE WELL VISIBILITY," filed October 22, 2002; (6) United States Patent Application Serial No. 10/278,393 ("the '393 application"), entitled "COLOR DISPLAY HAVING HORIZONTAL SUB-PIXEL ARRANGEMENTS AND LAYOUTS," filed October 22, 2002; (7) United States Patent Application Serial No. 01/347,001 ("the '001 application") entitled "IMPROVED SUB-PIXEL ARRANGEMENTS FOR STRIPED DISPLAYS AND METHODS AND SYSTEMS FOR SUB-PIXEL RENDERING SAME," filed January 16, 2003, each of which is herein incorporated by reference in its entirety, novel sub-pixel arrangements are therein disclosed for improving the cost/performance curves for image display devices.

[03] For certain subpixel repeating groups having an even number of subpixels in a horizontal direction, the following systems and techniques to affect proper dot inversion schemes are disclosed and are herein incorporated by reference in their entirety: (1) United States Patent Application Serial Number 10/456,839 entitled "IMAGE DEGRADATION CORRECTION IN NOVEL LIQUID CRYSTAL DISPLAYS"; (2) United States Patent Application Serial No. 10/455,925 entitled "DISPLAY PANEL HAVING CROSSOVER CONNECTIONS EFFECTING DOT INVERSION"; (3) United States Patent Application Serial No. 10/455,931 entitled "SYSTEM AND METHOD OF PERFORMING DOT INVERSION WITH STANDARD DRIVERS AND BACKPLANE ON NOVEL DISPLAY PANEL LAYOUTS"; (4) United States Patent Application Serial No. 10/455,927 entitled "SYSTEM AND METHOD FOR COMPENSATING FOR VISUAL EFFECTS UPON PANELS HAVING FIXED PATTERN NOISE WITH REDUCED QUANTIZATION ERROR"; (5) United States Patent

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Application Serial No. 10/456,806 entitled "DOT INVERSION ON NOVEL DISPLAY PANEL LAYOUTS WITH EXTRA DRIVERS"; (6) United States Patent Application Serial No. 10/456,838 entitled "LIQUID CRYSTAL DISPLAY BACKPLANE LAYOUTS AND ADDRESSING FOR NON-STANDARD SUBPIXEL ARRANGEMENTS"; and (7) United States Patent Application Serial No. {Attorney Docket No. 08831.0056.01} entitled "IMAGE DEGRADATION CORRECTION IN NOVEL LIQUID CRYSTAL DISPLAYS WITH SPLIT BLUE SUBPIXELS".

[04] These improvements are particularly pronounced when coupled with sub-pixel rendering (SPR) systems and methods further disclosed in those applications and in commonly owned United States Patent Applications: (1) United States Patent Application Serial No. 10/051,612 ("the '612 application"), entitled "CONVERSION OF RGB PIXEL FORMAT DATA TO PENTILE MATRIX SUB-PIXEL DATA FORMAT," filed January 16, 2002; (2) United States Patent Application Serial No. 10/150,355 ("the '355 application"), entitled "METHODS AND SYSTEMS FOR SUB-PIXEL RENDERING WITH GAMMA ADJUSTMENT," filed May 17, 2002; (3) United States Patent Application Serial No. 10/215,843 ("the '843 application"), entitled "METHODS AND SYSTEMS FOR SUB-PIXEL RENDERING WITH ADAPTIVE FILTERING," filed August 8, 2002; (4) United States Patent Application Serial No. 10/379,767 entitled "SYSTEMS AND METHODS FOR TEMPORAL SUB-PIXEL RENDERING OF IMAGE DATA" filed March 4, 2003; (5) United States Patent Application Serial No. 10/379,765 entitled "SYSTEMS AND METHODS FOR MOTION ADAPTIVE FILTERING," filed March 4, 2003; (6) United States Patent Application Serial No. 10/379,766 entitled "SUB-PIXEL RENDERING SYSTEM AND METHOD FOR IMPROVED

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DISPLAY VIEWING ANGLES" filed March 4, 2003; (7) United States Patent Application Serial No. 10/409,413 entitled "IMAGE DATA SET WITH EMBEDDED PRE-SUBPIXEL RENDERED IMAGE" filed April 7, 2003, which are hereby incorporated herein by reference in their entirety.

[05] Improvements in gamut conversion and mapping are disclosed in commonly owned and co-pending United States Patent Applications: (1) United States Patent Application Serial No. Attorney Docket No. 08831.0057 entitled "HUE ANGLE CALCULATION SYSTEM AND METHODS", filed October 21, 2003; (2) United States Patent Application Serial No. {Attorney Docket No. 08831.0058} entitled "METHOD AND APPARATUS FOR CONVERTING FROM SOURCE COLOR SPACE TO RGBW TARGET COLOR SPACE", filed October 21, 2003; (3) United States Patent Application Serial No. {Attorney Docket No. 08831.0059} entitled "METHOD AND APPARATUS FOR CONVERTING FROM A SOURCE COLOR SPACE TO A TARGET COLOR SPACE", filed October 21, 2003; and (4) United States Patent Application Serial No. {Attorney Docket No. 08831.0061} entitled "GAMUT CONVERSION SYSTEM AND METHODS", filed October 21, 2003, which are hereby incorporated herein by reference in their entirety. All patent applications mentioned in this specification are hereby incorporated by reference.

BRIEF DESCRIPTION OF THE DRAWINGS

[06] The accompanying drawings, which are incorporated in, and constitute a part of this specification illustrate exemplary implementations and embodiments of the invention and, together with the description, serve to explain principles of the invention.

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[07] **FIG. 1** shows a conventional signal processing pathway for a standard display/monitor/television unit displaying a television signal thereon.

[08] **FIG. 2** depicts one embodiment of the present invention wherein a standard television signal is processed and shown on a display/monitor/television that shows a reduction in bandwidth within the unit.

[09] **FIG. 3** shows one embodiment of a display/monitor/television architecture built in accordance with the principles of the present invention.

[010] **FIG. 4** depicts one possible embodiment of an architecture implementing a multi-mode operation on a display made in accordance with the principles of the present invention.

[011] **FIG. 5** shows a possible video sync and data timing signals to help effect a proper centering for letter box viewing.

[012] **FIG. 6** shows one embodiment of a EDID circuit to help enable multi-mode operation of a display system as controlled by a personal computer or the like.

[013] **FIGS. 7 and 8** show two alternate embodiments of architectures to effect multi-mode operation of a display system made in accordance with the principles of the present invention.

[014] **FIG. 9** shows one embodiment of a pixel doubler made in accordance with the principles of the present invention.

[015] **FIG. 10** shows one embodiment of a line doubler made in accordance with the principles of the present invention.

[016] **FIGS. 11 and 12** show yet another embodiment of a line doubler made in accordance with the principles of the present invention.

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[017] **FIGS. 13 and 14** show yet another embodiment of a line doubler made in accordance with the principles of the present invention.

[018] **FIGS. 15 and 16** show a high level block diagram of an architecture that may support interpolation as well as data duplication and the effects of its output respectively.

[019] **FIGS. 17 and 18** show two embodiments of similar architectures, one that supports interpolation exclusively and another that supports interpolation and duplication modes.

[020] **FIGS. 19 and 20** show another embodiment of a interpolation/duplication block and one possible signal diagram respectively.

[021] **FIGS. 21 and 22** show yet another embodiment of a interpolation/duplication block and one possible signal diagram respectively.

[022] **FIGS. 23 and 24** show one embodiment of a two-channel input pixel interpolation block and a possible signal diagram respectively.

[023] **FIGS. 25, 26 and 27** show one embodiment of a line interpolation/duplication block and timing diagrams for its interpolation mode and its duplication mode respectively.

[024] **FIGS. 28 and 29** show two embodiments of a two-channel input interpolation block, one that performs same color sharpening subpixel rendering and one that performs cross-color sharpening respectively.

[025] **FIGS. 30 and 31** show one embodiment of a two-channel input interpolation block and a possible timing diagram respectively.

[026] **FIGS. 32 and 33** show yet another embodiment of a two-channel input interpolation block and a possible timing diagram respectively.

[027] **FIG. 34** shows an alternative embodiment to the system of FIG. 4.

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[028] **FIG. 35** shows an alternative embodiment to the system of FIG. 18.

[029] **FIG. 36** shows an alternative embodiment to the system of FIG. 25.

[030] **FIG. 37** shows one possible timing diagram for the system of FIG. 36.

[031] **FIG. 38** shows an alternative embodiment to the system of FIGS. 25 and 36.

[032] **FIGS. 39 and 40** show possible timing diagrams for interpolation mode and duplication mode for FIG. 38.

DETAILED DESCRIPTION

[033] Reference will now be made in detail to implementations and embodiments, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[034] Currently, there are a number of television broadcast standards in existence and several companies have attempted to create display systems that are capable of receiving a number of such broadcasts and rendering them onto a common display.

[035] Figure 1 is typical of some of the image processing pathways through these multi-mode displays. Pathway 100 starts by inputting one of any number of standard television signals at 102 – possibly in need of de-interlacing picture processing at 103. As one example, the signal could be NTSC in 640x480 RGB format – i.e. having 640x3x480 resolution. An image processing block 104 accepts this data and upsamples the data to 1280x3x960 data for rendering on, for example, an RGB striped 1280x3x960 display. The signal leaving image processing block 104 is at approximately "high definition television" (HD) bandwidths and is input into at

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video processing block 106, which typically incorporates frame buffers at approximately 1280x3x960 dimensioning. Any desired auxiliary for the display system – such as subpixel rendering, response time enhancement, or other image enhancement function – could be performed by the video processing block. The output of video processing block 106 is again of the order of HD bandwidth – which is received as, for example, 1280x960 input into the aforementioned display.

[036] In accordance with the principles of the present invention, however, Figure 2 shows one embodiment of a different image processing pathway that can occur to give similar image rendering performance – but with reduced memory and bandwidth requirements. Pathway 200 could accept one of any number of standard television signals at 202 (e.g. the same NTSC signal as in Figure 1). This signal is of the order of NTSC bandwidth and is input into an optional de-interlacing picture processing block 204 (if de-interlacing is required of the signal). The output of this block is again of the order of NTSC bandwidth and is subsequently input into an interpolation/subpixel rendering (SPR) block 206.

[037] As will be further discussed below and as is further detailed in the co-pending related applications herein incorporated by reference, the interpolation/SPR block 206 does not need multiple frame buffers at 1280x3x960 dimensioning. Additionally, the signal that is output to the display 208 is on the order of one half of the bandwidth associated with HD – even though the rendered image is of HD quality. This is possible, in part, because display 208 employs one of a number of novel subpixel layouts disclosed in many of the commonly assigned applications incorporated by reference above.

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[038] Figure 3 shows one possible embodiment of an architecture as made in accordance with the principles of the present invention. Display system 300 accepts one of a plurality of analog and/or digital signals for multi-mode processing – for example, NTSC, VGA or SXGA RGB data, HDTV, and other formats. The signal is fed into the interpolation and/or SPR block 302 where the input data may be appropriately scaled and subpixel rendered for display. In this example, the output of block 302 may be input into a timing controller 304 – however, it should be appreciated that, in other embodiments, the interpolation and SPR may be incorporated into the timing controller itself, may be built into the panel (particularly using LTPS or other like processing technologies), or may reside elsewhere in the display system (e.g. within a graphics controller). The scope of the present invention should not be particularly limited to the placement of the interpolation and/or subpixel rendering within the system.

[039] In this particular embodiment, the data and control signals are output from timing controller 304 to column drivers 306 and row drivers 308. Data is then sent to the appropriate subpixels on display panel 310. As shown here, panel 310 is formed by a substantially repeating subpixel grouping 312, which is comprised – as seen in an expanded view – of a 2x3 subpixel unit wherein vertical striped subpixel 314 depicts the color red, horizontal striped subpixel 316 depicts the color blue, and the diagonally striped subpixel 318 depict the color green. It should be appreciated that the subpixels in repeating group 312 are not drawn to scale with respect to the display system; but are drawn larger for ease of viewing. One possible dimensioning for display 310 is 1920 subpixels in a horizontal line (640 red, 640 green and 640 blue subpixels) and 960 rows of subpixels. Such a display would have the requisite number of subpixels to display VGA, 1280x720, and 1280x960 input signals thereon.

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[040] Table 1 below is a summary of the possible display systems comprising panels having subpixel resolutions – e.g. 640x3x960 would indicate a panel having 640 red, 640 green and 640 blue subpixels in a row, comprising 960 such rows. Such a panel used in the present invention would have an effective maximum resolution of 1280x960 – wherein each red and green subpixel could effectively be the center of luminance for an RGB pixel value. The last column indicates some of the modes that such a display system of the present invention could then support. For example, the above described panel and system could support VGA, SVGA, NTSC, PAL and 720p video formats.

Table 1

Subpixel resolution	Effective max resolution	Supported modes
640x3x960 (4:3)	1280x960	VGA (1:2), SVGA, NTSC, PAL, 720p (1:1)
640x3x1024 (5:4)	1280x1024	VGA, SVGA, XGA, SXGA (1:1), NTSC, PAL, 720p
960x3x1080 (16:9)	1920x1080	WVGA, WXGA, 720p, 1080i (1:1)
852x3x960 (16:9)	1704x960	WVGA (1:2), WXGA
1280x3x1440 (16:9)	2560x1440	WXGA (1:2), 720p, 1080i

Note: Possible aspect ratio included in column 1, and possible scaling ratio in column 3

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[041] As further disclosed in the related patent application incorporated herein, displaying a standard 640X480 television signal onto a panel as discussed herein – i.e. one that comprises 640 X 3 X 960 physical subpixels; but has greater image quality with subpixel rendering -- may take advantage of interpolation followed by cross-color sharpened subpixel rendering to effectively scale the image to 1280 X 960 logical pixels. This reconstructs the image with reduced moiré and aliasing artifacts since the interpolation serves as a low-pass reconstruction filter for the luminance signal while the sharpened subpixel rendering filter serves to remove any spatial frequencies that may cause chromatic aliasing, thus preserving the color balance and image constrast.

[042] Also, shown in Figure 3, other subpixel repeating groups 320, 322, 323, 324, 325 and 326 are also possible for purposes of the present invention. These subpixel repeating groups and algorithms to drive them are further disclosed in the above applications incorporated by reference. The subpixel repeating group 320 depicts use of at least a fourth color -- e.g. white, cyan, blue-grey, magenta or the like -- which could expand the color gamut and/or brightness of the display over and above traditional 3 color primary systems. The other subpixel repeating groups could similarly comprise at least a fourth color as well. As with some of these subpixel repeating groups, the bandwidth and memory requirements are in a range that is less than what traditional RGB stripe systems require, and down to approximately one half of HD bandwidth. One of the reasons is the subpixel rendering as disclosed in the '612 application, the '355 application, and the '843 application boosts the effective resolution of the panels with these novel layouts in both horizontal and vertical axes. Thus, the subpixels in question may be resized to (for example) a 2:3 aspect ratio, as opposed to the standard 1:3 aspect ratio found in traditional RGB stripe displays. This resizing creates a display panel of comparable image

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display quality; but with approximately one half the number of subpixels in a horizontal direction. This reduces the bandwidth and memory requirements appropriately.

[043] Figure 4 shows one possible embodiment of a present interpolation/SPR block 302. Block 302 is depicted here as one that may optionally support a multi-mode (i.e. accepts multiple video input formats and displays one or more output video formats) operation. It will be appreciated that, although Figure 4 shows particular resolution specification numbers and other implementation details, these details are meant for illustrative purposes only and the present invention is not to be limited to particular numbers or formats specified in the Figures.

[044] Input signal 402 arrives at interpolation/duplication block 404 and an input resolution detector 406. As shown for illustration purposes, signal 402 could be 640x480 or 1280x960. Two pathways (Path A and B) are shown as one embodiment of multi-mode support. If the detector 406 detects the signal as a 1280x960 signal, then the interpolation/duplication block 404 is bypassed -- e.g. by either disabling the block or, as shown, using a MUX 408 to select an alternate data path (e.g. Path B) for input into the SPR block 410.

[045] Interpolation/duplication block 404 could be implemented, as one embodiment, to either use interpolation (e.g. linear, bi-linear, cubic, bi-cubic and the like) or duplication (i.e. replicate horizontal pixel data to expand from 640 to 1280 pixel values and replicate line data to expand from 480 to 960 line values) to achieve appropriate scaling. It will be appreciated that other embodiments could employ either only interpolation or only duplication as opposed to having a choice among the two modes. In this embodiment, a doubling (interpolation or duplication) mode signal 412 could be supplied to block 404 and to a MUX 414 to select the appropriate filter kernel to the SPR block 410.

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[046] Three such filters are shown 416, 418, 420 for illustrative purposes. Filter 416 could be a "unity" filter – which could be used with VGA input and in a duplication mode. Such a unity filter could be implemented with the following coefficients for all colors (R, G and B):

$$\begin{matrix} 0 & 0 & 0 \\ 0 & 255 & 0 \\ 0 & 0 & 0. \end{matrix} \quad \times 1/255$$

[047] Filter 418 could be a "sharpening" filter, designed to give improved image quality for video data; and could possibly be used for VGA input with an interpolation mode. One such sharpening filter might be implemented (for R and G colors) as:

$$\begin{matrix} -16 & 32 & -16 \\ 32 & 192 & 32 \\ -16 & 32 & -16. \end{matrix} \quad \times 1/255$$

[048] Filter 420 could be a "diamond" filter, designed to give improved image quality for text image data and could possibly be used for SXGA input. One such diamond filter might be implemented (for R and G colors) as:

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0 32 0

32 128 32 x 1/255

0 32 0.

[049] The blue color for the last two filters could be implemented as:

0 0 0

0 128 128 x 1/255

0 0 0.

[050] A fourth filter 421 is shown to depict that N filters could be possibly employed by the subpixel rendering block. Such other filters might implement area resampling or a windowed sync function. As mentioned, the choice of which filter to apply could be determined by select signals applied to a MUX 414 with the select signals being a duplication (or interpolation) mode select signal and an input resolution detection signal. The duplication or interpolation mode select signal could be supplied by the user of the display system (e.g. depending upon whether the user wants to display primarily video or text images) or the select signal could be supplied by applications that are accessing the display system and are capable of automatically deciding which mode and/or filter to apply depending upon the state of the application.

[051] Once subpixel rendering has occurred, the video output data can be supplied upon a Video Out line 422 and the sync signals could also be optionally sent to an optional centering sync block 424. Centering sync block 424 could supply an output sync signal 428 depending

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upon the data (e.g. 640x480 or 1280x960) format being output. If the output data is 1280x960, then output display image does not need to be centered – e.g. as in a letter box format. If the input is 1280x720, it might be desirable to pad the scaled signal to be centered by appropriate introduction of black lines before and after the 720 active lines of data.

[052] Figure 34 is an alternative embodiment for the system of Figure 4. In Figure 34, the Input Resolution Detector sets a "bypass" signal and supplied to the Interpolation/Duplication block so that input signals may be passed through to the SPR block directly – in either serial (depending upon whether buffers are employed in SPR block) or via three data lines. Figure 35 shows another embodiment of the present system which employs the bypass signal at a Mux 3502 and at Line Select to effect one possible bypass mode. Figure 36 shows yet another embodiment in which bypass mode is effected to supply data on lines 3602, 3604 and 3606 for such bypass mode of operation. Figure 37 is one possible timing diagram for the bypass mode of Figure 36.

[053] Figure 38 is one embodiment of the present system that may be used in the Interpolation/Duplication block of Figure 4. A single Line Out may supply data to the SPR block that may, in turn, buffer the data. Figures 39 and 40 show possible timing diagrams for the Interpolation Mode and Duplication Mode respectively for the system of Figure 38.

[054] Figure 5 depicts the effect of applying the appropriate black line padding to a 640x480 scaled output signal for display – e.g. having 1280x1024 subpixels and displaying scaled VGA 1280x960 output data. As may be seen, the centering sync signal could be used to take a video stream bordered by a back porch (BP) delay and a front porch (FP) delay plus 64

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lines to create a video stream that has the appropriate BP and FP delays that have a more equal distribution of padded black lines to center the image data on the display.

[055] Figure 6 depicts another optional aspect of the present invention. EDID selection circuit 600 could be implemented to inform another system – e.g. a personal computer (PC) or the like – regarding the display resolution capabilities of the display system. Typically in a display system, EDID comprises a plurality of ROM storage (e.g. 606 and 608 and possible other ROMS that are not shown) that informs a PC or other suitable system what the display capabilities are of the display via an I2C communications channel 610. In a multi-mode display system, however, it may be important for the user or application accessing the display system to inform the PC or the like what the capabilities are and either could select (602) which signal to send to MUX 604. Once the proper EDID data is selected (e.g. as shown VGA or SXGA or any other ROM to enable other modes as necessary), such data would be supplied to the PC via a graphics card or the like.

[056] Other embodiments of the present system are shown in Figures 7 and 8. Figure 7 shows a system 700 that accepts a plurality of input signals at MUX 702 and depending upon what resolution detector 704 detects, the input data is sent to a plurality of paths (only two shown here as 480p or 720p data – of course, other data and their paths are possible). Each path may be sent into an SPR block (shown here as a 1:2 SPR and 1:1 SPR 714, 716 respectively – of course, other SPR blocks that implement different scaling modes are possible). Depending upon the resolution of the input data set, the system could add lines (708) or double the number of lines (710), and possibly provide a centering block (712) for one or more resolution modes. The results of the SPR blocks may be multiplexed (718) according to which data is to be rendered

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upon the display 722. Likewise, the line signals may be multiplexed (720) according to which data is to be rendered on the display. Figure 8 is yet another embodiment of the present system that is similar to Figure 7. One difference is that a reduced number of SPR blocks are used in the system because one or more input data paths are interpolated (802) to provide a correct amount of data to the SPR blocks.

[057] Now it will be shown some embodiments suitable to perform some desired interpolation upon image data. Figure 9 depicts a pixel doubler block 900 that takes input data 902 and latches the input (904). Multiplies 906, adder 908 effect the cubic interpolation scheme mentioned above. It should be appreciated that the given coefficients allow cost effective computation – for example, a divide by 1/16 is a right shift four times and multiplying by 9 can be done with a left shift three times and an add with the original value. On even outputs, one of the input pixels is output directly, on odd outputs, the interpolated value is produced – with even and odd outputs effected by Mux 910.

[058] Figure 10 shows one embodiment of an odd line doubler 1000. Odd line doubler inputs image data 1002 (as shown as a plurality of input lines of 640 pixels each – of course, other line widths are possible for other image data formats), and sends the pixel data to a pixel doubler (e.g. the one disclosed in Figure 9 or the like) which doubles the width of the line. Three doubled lines are stored into line buffers 1004 (for another cubic interpolation step) and one is buffered 1006 so that the appropriate data is present in the multipliers 1008 and adder 1010 to produce the vertical interpolation. This interpolates between lines 2 and 3. It should be noted that only the last 3 of these values need to be saved in latches 1012 – since those 3 (plus 3 values

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from line 2 above and 3 values from line 3 below are stored in 1012) are desired to do subpixel rendering (SPR) 1014.

[059] It should also be noted that SPR may be done with two line buffers. Combining cubic interpolation with SPR removes the requirement of separate line buffers. An additional line buffer is all that may be needed to do the cubic interpolation. It should additionally be noted that even with SPR, one more line buffer may be added to synchorize the input and output video streams. So, while typical SPR may require a total of 3 line buffers, the present system may make use of 4 line buffers to effect line doubling and cubic interpolation-SPR.

[060] Figures 11 and 12 shows yet another embodiment of a full line doubler 1100 and 1200 respectively. Figure 11 shows a system for generation even lines 1100. Because the system outputs twice as many lines as it inputs, Figure 11 shows the line buffers 1102 being recirculated such that the odd lines are generated with no new input pixels via multipiers 1104 and adders 1106. Line 2 is output directly to the latches 1108 for SPR and two new interpolated lines are generated – one between Line 1 and 2 and another between Line 2 and 3.

[061] Figure 12 shows a system 1200 for generating the odd lines. Pixel doubler 1202 produces horizontally interpolated values which are stored in line buffers 1204. Lines 1-4 output to multipliers 1206 and adder 1208, similar to that shown in Figure 10. The output from adder 1208 plus the direct output from lines 2 and 4 are shifted through latches 1210 to supply the values desired for SPR. Line 4 could also serve as the synchorization buffer as discussed above. Line 0 is employed for saving the data to be used on the even lines as discussed in Figure 11 above.

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[062] Figures 13 and 14 are yet another embodiment of a full line doubler. Figure 13 shows an odd line doubler 1300. Pixel doubler 1302 inputs data to a plurality of line buffers 1304. Lines 1, 2, 3 and 4 are vertically interpolated to produce the center line of data stored in latches 1310. The output from the adder 1308 is recirculated into a line between Line 1 and 2, and called Line 1A. The output of Line 2 and Line 3 are directly input into latches 1310 for SPR. Figure 14 shows the even line doubler 1400 where the line bufferes 1402 are recirculated. Lines 1, 2, 3 and 4 are input into multipliers 1404 and adder 1406 to perform vertical interpolation, with the results input into the last buffer of 1408 for SPR. Lines 1A and 2 are directly input into latches 1408. It should be noted that the line buffers in Figures 13 and 14 may be shared between the even and odd doublers. During the odd line output, Line 1A is filled in Figure 13 and that line is used in the even lines in Figure 14. It should also be noted that the use of Line 1A buffer in Figures 13 and 14 obviate the need of the extra multiply/adder as shown in Figures 11.

[063] Figures 15 and 16 depict yet another embodiment of an interpolation block that may support both interpolation and duplication schemes. In an embodiment that effects multiple modes of resolution, two schemes – interpolation and/or duplication – may be used to effect these modes. For example, if the input resolution is 640x480, it is possible to use either interpolation or duplication to output 1280x960 resolution. Both interpolation and duplication have their own unique properties – interpolation generally makes images smoother; while duplication tends to keep images sharper than interpolation. It is possible to effect interpolation and duplication in one processing block for a more cost effective system. Figure 15 shows a high level block diagram 1500 of such a system. Video input 1502 is input into interpolation filter 1504 which effects an interpolation scheme (such as the one discussed above). One line of video

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input, however, bypasses the interpolation block and is supplied at the input of mux 1506. Depending upon whether interpolation or duplication is desired (via Mode select), the output of the mux is shown in Figure 16.

[064] Figures 17 and 18 depict how to migrate from a strictly interpolation block 1700 having a pixel interpolation unit 1702 and a line interpolation unit 1704 into a dual interpolation/duplication block 1800. Dual mode block 1800 has similar pixel interpolation and line interpolation blocks as in Figure 17; but with the addition of two Muxs 1804 and 1806. These two Muxs are supplied a mode select signal that selects either the interpolation or the duplication mode.

[065] Figures 19 and 20 show one embodiment of a pixel interpolation block of Figure 18. As shown, video data is input into a plurality of latches and subsequently sent to multipliers/adder to effect interpolation. Bypass 1902 is used, however, to effect pixel doubling via Mux 2 upon an appropriate mode select signal. Figure 20 shows one possible signal timing diagram for the embodiment of Figure 19. Figures 21 and 22 shows an alternative embodiment of the pixel interpolation block with its associated timing diagram.

[066] Figures 23 and 24 depict one embodiment of a two-channel input pixel interpolation block 2300. Video Output A is a bypass mode to allow for native input data to bypass the processing in block 2300. Video Output B is an output selected by Mux2 depending upon a mode select signal. It should be noted that there are opportunities to efficiently design block 2300 to remove the need of a multiplier, as seen in Figure 23. Figure 24 shows a possible timing diagram of the block of Figure 23.

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[067] Figures 25, 26 and 27 depict one embodiment of a line interpolation block, with timing diagrams for interpolation mode and duplication mode respectively. As may be seen from Figure 25, Line Mux selects either interpolated lines or duplicated lines depending upon its mode select signal. The timing diagrams of Figure 26 and 27 show the respective operations of this block. The Line Select operation is as follows: during odd line, Line Out1 is Line Buffer5 output, Line Out2 is Line buffer2 output, and Line Out3 is Line MUX output; during even line, Line Out1 is Line buffer2 output, Line Out2 is Line MUX output, and Line Out3 is Line buffer3 output.

[068] Figures 28 and 29 are two embodiments of a two-channel input interpolation block, one that may perform same color sharpening subpixel rendering (SPR) and one that may perform cross-color sharpening SPR, respectively. In Figure 29, red and green image data are provided to red SPR and green SPR units together to perform the cross-color sharpening subpixel rendering.

[069] Figure 30 shows one embodiment of a two-channel input interpolation block. As may be seen in Figure 30, five input pixels input data into two interpolation units (i.e. multipliers and adder) and two outputs – Video Output A and B -- are presented. As may be seen in one possible timing diagram of Figure 30, Video Output A outputs the native mode input data while Video Output B outputs the interpolated data

[070] Figure 32 shows yet another embodiment of a two-channel input interpolation block. As may be seen, the embodiment of Figure 32 uses only three data latches, as opposed to five data latches used in Figure 30. Figure 33 shows a possible timing diagram of the block shown in Figure 32.

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[071] While the invention has been described with reference to an exemplary embodiment, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.

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